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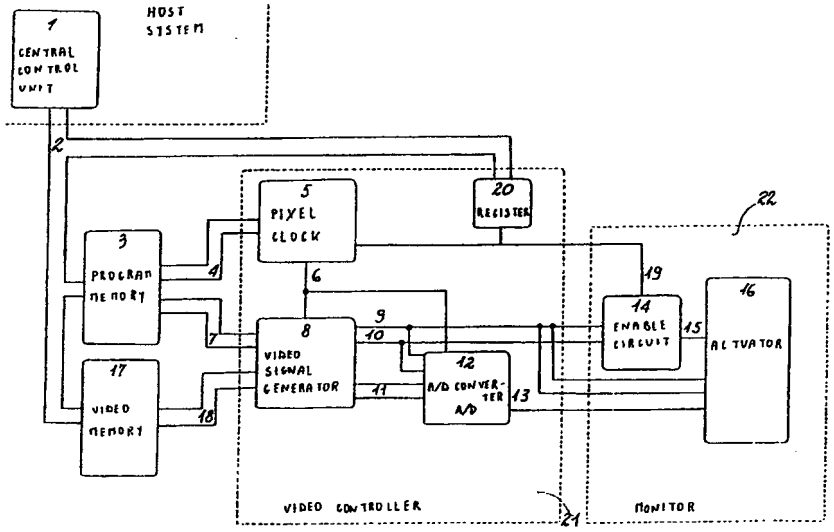
(54) Title: VIDEO DISPLAY FOR DIGITAL IMAGES AT HIGH FREQUENCY OF FRAME REFRESH



(57) Abstract

The device enables to visualize the images registered in the video memory on the base of standard modes guaranteeing the compatibility with such informatic standards and improving the ergonomic characteristics of the display. The device consists of an intelligent programmable video controller (21) which generates the data and control signals for the cathode-ray tube monitor (22). The number of pixels on each line and the number of lines on each frame are defined by the standard graphics for Personal Computers, named VGA. Such standard is foreseen to use a frequency for frame refresh under 60 Hz for the resolution graphic modes (640 pixels for 480 lines) and equal to 70 Hz for the text modes. The invention device enables to obtain frame refresh frequency above 70 Hz for whatever mode, while respecting the compatibility with the standard VGA, by means of speeder pixel clocks (27 and 28), of the circuitry (5) used to select them, as well as for the monitor (22) capable of synchronizing on the frequencies generated for the ergonomic mode.

* See back of page

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"Video display for digital images at high frequency of frame refresh".

The present invention concerns a device able to display digital images formed by pixels ordered on lines and columns on an intelligent screen. This visualization consists of a set of pixel signals, characterized by the horizontal and vertical scanning frequency on the screen, according to pre-fixed resolutions on the base of the contents of a video memory which is periodically read by the pixel signal generator. The video controller includes a series of registers which must be programmed with the proper parameters according to the chosen type of resolution. The video contains the mechanisms for the horizontal and vertical synchronization and sweep, in order to synchronize on the pixel signal, generated by the video controller, and consequently to position the cathode-rays gun in the right position on the screen.

There are many video displays of the above described type. Some of such video controllers which use particular resolutions, a certain set of programmable registers and a video memory structured according to exact access mode, became a standard in the industrial branch of the personal computer.

For these controllers a very large number of programs and applications has been developed with reference to them and, therefore it is essential for a personal computer to offer the compatibility with this "de facto standard". One of the most powerful and diffused standard is called VGA. The technical problem resolved by the present invention is to improve the visual characterists of th image on the screen, still respecting the need of compatibility due to the VGA standard. There are many parameters that define the quality of the video image, and one of the most important is the frequency of the frame refresh. This frequency determines the time between two subsequent passages of the electron beam on the same point of the screen. More frequent is this passage, more stable the immage appears to the eye of the observing operator, thus reducing the wear of the retina and of whole view apparatus.

The device is expressed through the operational components which operate in the numeral sequence of table 1. Through the communication channel of data and addresses 2, the central control unit 1 of the host system accesses to register 20 and gets the information on the monitor type to determine the program sequences to use for programming the timing registers of the video controller. Consequently, the said unit 1 accesses the program memory 3, to activate the program sequences 4 which inform the circuit of pixel clock selection 5. This circuit, on the base of this information as well as of the identification signal 19 coming from the monitor 22, selects the pixel clock 6, which will temporize the operations of the video signal generator 8 and of the digital-to-analog converter of the video signal 12. The same central control unit 1 of the host system, through the same communication channel of data and addresses 2, accesses to the same program

memory 3 to activate the sequences of program 7, which, with the programming sequences required by the set video mode, initialize the registers of the video signal generator 8. This video signal generator 8 scans the video memory 17, previously filled by the central control unit 1 through the data and addresses channel 2, to obtain the information through the data and addresses channel 18. The same video signal generator 8 will transform these information into digital video signals and will put them on the data channel 11 towards the D/A converter 12, as well as will generate the horizontal 9 and vertical 10 sync signal which are sent both to the D/A converter 12, to interprete the data flow of channel 11, to the mode detector circuit 14, which stays in the video module, and to the circuitry of the monitor. For the timing of the video signals and synchronisms the video signal generator 8 will use the pixel clock 6 as the time base, and the contents of its timing registers, which are programmed by the program sequences 7, will define the characteristics of these timings. The mode detector circuit 14 arranges to generate the information 15 for the synchronization circuits and for the actuators of the cathode-ray beam 16, in order to select the operation of higher frequences than the standard one.

A preferred execution form of the circuit for the pixel clock selction is represented in table 2, for an exemplifying but not limiting purpose. Through the data and addresses channel 4, the selction register 23 for the ergonomic or the standard VGA mode is initialized. The coincidence (logical AND) of the information coming from the register 23 and of the identification signal 19 coming from the monitor, which indicates whether the monitor is able to support the high frequency refresh mode, is sent on the INPUT selection

signal (A/B) of the MULTIPLEXER 24. The MULTIPLEXER 24 in INPUT has the standard clocks 25 and 26, respectively like 25,275 MHz and 28,322 MHz, and the speeder clocks 27 and 28 used for the ergonomic mode. On the OUTPUT lines 29 and 30 the MULTIPLEXER 24 selects the pixel clock for the alpha-numerical and graphic modes which have different horizontal resolutions and, therefore, different pixel clocks. It must be noted that the monitor, through the identification signal 19, will state to the video controller that it can to support the ergonomic mode, when it is able to accept two horizontal frequences equal to 31,5 KHz, standard VGA frequency and at least 35,5 KHz required for the ergonomic VGA mode. The pixel clocks 29 and 30 become the INPUT for a second MULTIPLEXER 31 which in OUTPUT selects the pixel clock 6 on the base of the INPUT selection signal coming from the register 32 which is programmed through the data and addresses channel 4 and which indicates whether the current mode is alpha-numerical or graphic.

Alternatively, the register 32 could be replaced by a register which memorizes the information of a user accessable switch, who selects between standard VGA video mode and ergonomic VGA video mode.

The present device is illustrated in a merely indicative way by the drawings of the tables 1 and 2. With reference to these tables, fig. 1 is the scheme of the different operative components, whereas fig. 2 is a preferred execution form for the selection circuit of pixel clock 5.

Claim.

1) Video display for digital images at high frequency of frame refresh, characterized by the fact that through the communication channel of data and addresses (2) the central control unit (1) of the host system accesses to register (20) and gets the information on the monitor type to determine the program sequences to use for programming the timing registers of the video controller. Consequently, the said unit (1) accesses the program memory (3) to activate the program sequences (4) which inform the circuit of pixel clock selection (5). This circuit, on the base of this information as well as of the identification signal (19) coming from the monitor (22), selects the pixel clock (6), which will temporize the operations of the video signal generator (8) and of the digital-to-analog converter of the video signal (12). The same central control unit (1) of the host system, through the same communication channel of data and addresses (2), accesses to the same program memory (3) to activate the sequences of program (7), which, with the programming sequences required by the set video mode, initialize the registers of the video signal generator (8). This video signal generator (8) scans the video memory (17), previously filled by the central control unit (1) through the data and addresses channel (2), to obtain the information through the data and addresses channel (18). The same video signal generator (8) will transform these information into digital video signals and will put them on the data channel (11) towards the D/A converter (12), as well as will generate the horizontal (9) and vertical (10) sync signal, which are sent both to the D/A converter (12), to interprete the data flow of channel (11), to the mode detector circuit (14), which stays in the video module, and to the circuitry of the

monitor. For the timing of the video signals and synchronisms, the video signal generator (8) will use the pixel clock (6) as the time base, and the contents of its timing registers, which are programmed by the program sequences (7), will define the characteristics of these timings. The mode detector circuit (14) arranges to generate the information (15) for the synchronization circuits and for the actuators of the cathode-ray beam (16), in order to select the operation ot higher frequences than the standard one.

AMENDED CLAIMS

[received by the International Bureau on 30 July 1991 (30.07.91)
original claim 1 replaced by amended claim 1 (2 pages)]

1) A video display adapter for displaying digital images at high frequenciey of frame refresh, associated to the communication channel (2), for data and addresses of a central control unit (1) of a host system, arranged to have a register (20) to get information to determine the program sequences for programming timing registers of a video controller, said unit (1) having access to the program memory (3) to activate the program sequences (4) which inform the circuit (5) for pixel clock selection, said circuit (5) on the basis of such information as well as of an identification signal (19) coming from a monitor (22) selecting the pixel clock (6), which well give timing of the operations of a video signal generator (8) and of a digital-to-analog converter (22) for the video signal, said central control unit (1) of a host system, through the same communication channel of data and addresses (2) having access to said program memory (3) for activating the sequences of program (7), which, with the programming sequences required by the set video mode, initializes the registers of said video signal generator (8), said video signalgenerator performing the scanning of a video memory (17), previously filled by said central control unit (1) through said data and addresses channel (18), said video signal generator (8) being arranged to transform this information into digital video signals put on a data channel (11) towards the D/A converter (12), as well as to generate horizontal (9) and vertical (10) synchronism signals, both sent to said D/A converter (12), to interprete the data flow of channel (11), to a mode detector circuit (14), located in a video module, and to the circuitry of the monitor (16); the timing of the video signals and synchronisms, the video signal generator (8) being controlled by the pixel clock (6) as time base, and the contents of its timing registers, which are programmed by the program sequences (7), defining the characteristics of these timings, said mode detector circuit

(14) being arranged to generate the information (15) for the synchronization circuits and for the actuators of a cathode-ray display (16), in order to select the operation at higher refresh frequencies than the standard ones.

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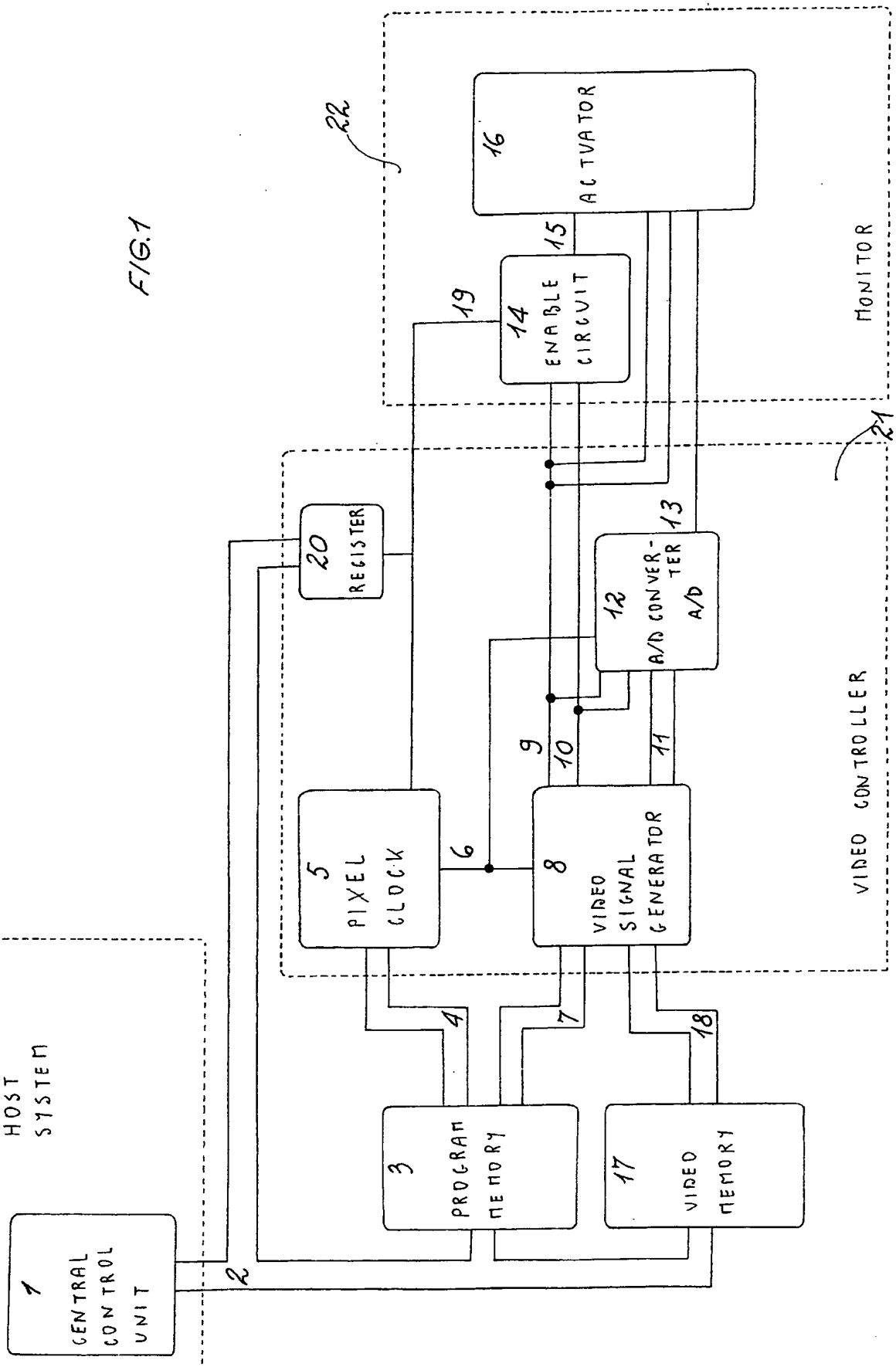
FIG.1



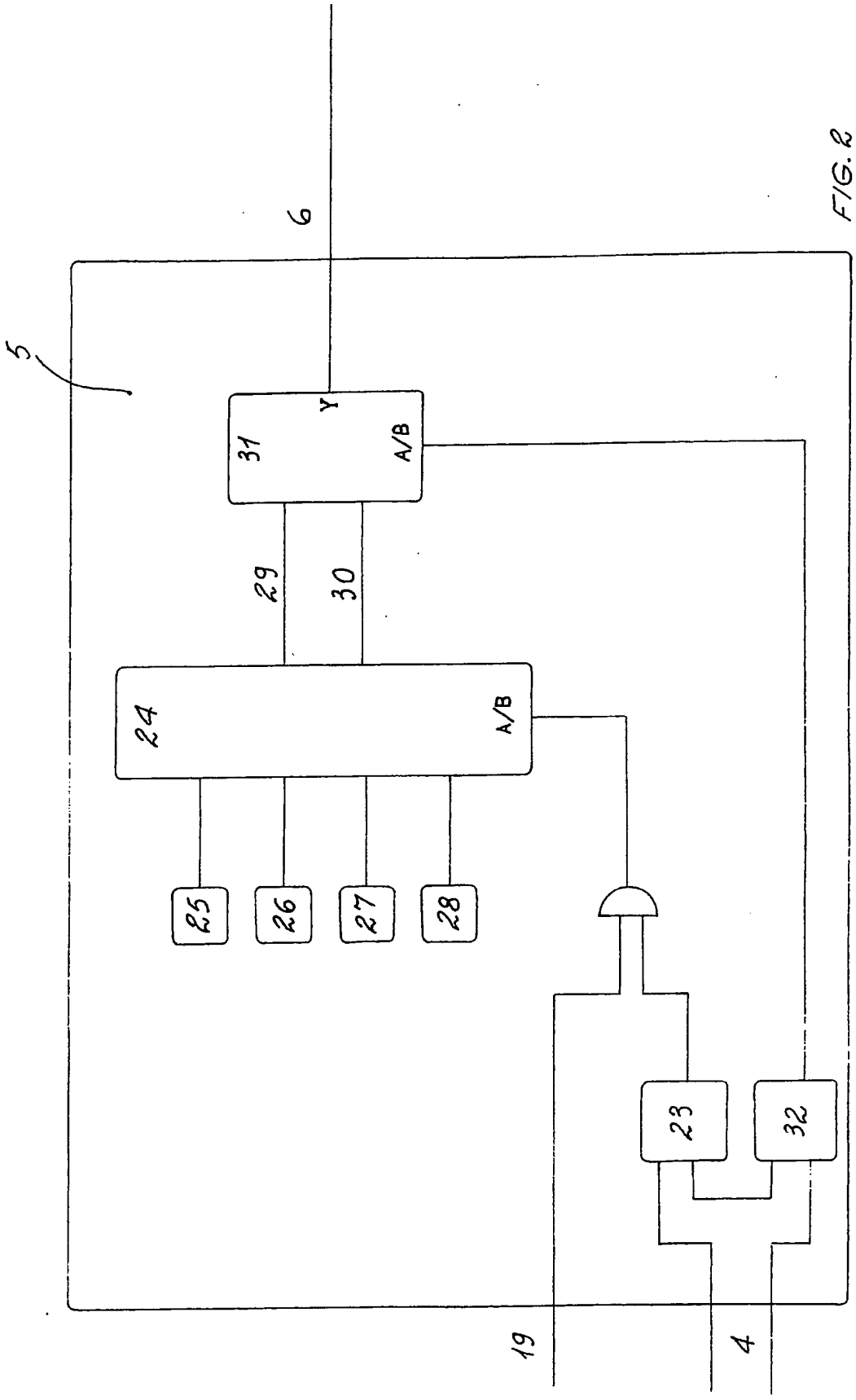


FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No PCT/IT 90/00036

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[5]: G 09 G 1/16

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[5]	G 09 G

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	IBM Technical Disclosure Bulletin, volume 29, no. 11, April 1987, IBM Corp., (Armonk, NY, US), "Programmable dot clock for video adapter", pages 4859-4860 see the whole article	1
A	Research Disclosure, no. 256, August 1985, Emsworth, (Hampshire, GB), "Monitor-type sensing circuit" page 414 see the whole article	1
A	US, A, 4616260 (DOUGLAS A. ERWIN) 7 October 1986 see abstract; column 2, lines 5-32	1
A	US, A, 4905167 (SHIGEMITSU YAMAOKA) 27 February 1990 see abstract; column 2, lines 3-35	1

* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
20th November 1990	18. 12. 90
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	H. Ballesteros

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ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO. IT 9000036
SA 35856

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4616260	07-10-86	None	
US-A- 4905167	27-02-90	JP-A- 63147189	20-06-88